- - REMARKS - -

The present amendment replies to a First Non-Final Office Action dated June 19, 2002. Claims 1-9 are currently pending in the present application.

The Applicant has amended the specification herein to correct each detected typographical/grammatical error and inadvertent omission in the specification. Attached hereto is a marked-up version of the amendment to the specification that is captioned "**Version With Markings To Show Changes Made**". No new matter has been introduced by the amendment of the specification.

The Applicant has amended claims 1-5, 8 and 9 to correct each format/typographical/grammatical error in claims 1-5, 8 and 9. Attached hereto is a marked-up version of the amendment to claims 1-5, 8 and 9 that is captioned "**Version With Markings To Show Changes Made**". No new matter has been introduced by the amendment of claims 1-5, 8 and 9.

In the First Non-Final Office Action, Examiner Baker rejected claims 1-9 under 35 U.S.C. §103(a) as being unpatentable over Dallas Semiconductor *DC87C550 Data Sheet* in view of U.S. Patent No. 5,416,769 to *Palowski*. The Applicant has thoroughly considered Examiner Baker's remarks concerning the §103(a) rejection of independent claim 1, and carefully reviewed both the *DC87C550 Data Sheet* and the *Palowski*. The Applicant respectfully traverses the §103(a) rejection as subsequently recited herein, and respectfully requests reconsideration and further examination of the present application under 37 CFR §1.112.

As to the traversal, *Palowski* teaches an Expanded Data Memory 802 (FIG. 8) having a control SFR that is programmed for enabling or disabling an auto-increment and auto-decrement functions of an address SFR. *Palowski* fails to explicitly teach how the control SFR is programmed to perform this task.. However, *Palowski* does teach that the programming of the control SFR is performed prior to an execution of instructions within a code segment for swapping of the nibbles of a buffer. Thus, *Palowski* fails to disclose, teach or suggest the control SFR of *Palowski* being programmed as a side effect of an execution of an instruction. See, *Palowski* at column 14, line 22 to column 15, line 30.

By comparison, the control register recited in independent claim 1 is "instruction-settable to respective control states that control whether or not the processing device updates that at least two address as a side-effect of executing the memory access instruction". Examiner Baker has correctly recognized that the DC87C550 data processing device of *DC87C550 Data Sheet* does not include a control register as recited in independent claim 1. Thus, neither *DC87C550 Data Sheet* nor *Palowski* discloses a "control register that is instruction-settable to respective control states that control whether or not the processing device updates that at least two address as a side-effect of executing the memory access instruction" as recited in independent claim 1. Withdrawal of the rejection of independent claim 1 under 35 U.S.C. §103(a) as being unpatentable over *DC87C550 Data Sheet* in view of *Palowski* is therefore respectfully requested.

Claims 2-9 depend from independent claim 1. Therefore, dependent claims 2-9 include all of the elements and limitations of independent claim 1. It is therefore respectfully submitted by the Applicant that dependent claims 2-9 are allowable over *Roux* for at least the same reason as set forth with respect to independent claim 1. Withdrawal of the rejection of dependent claims 2-9 under 35 U.S.C. §103(a) as being unpatentable over *DC87C550 Data Sheet* in view of *Palowski* is therefore respectfully requested.

SUMMARY

Examiner Baker's 35 U.S.C. §103(a) rejection of claims 1-9 have been obviated by the above remarks. The Applicants respectfully submit that claims 1-10 fully satisfy the requirements of 35 U.S.C. §§ 102, 103 and 112. In view of the foregoing, favorable consideration and early passage to issue of the present application is respectfully requested.

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Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The paragraph beginning on page 1, lines 9-17 has been amended as follows:

"The original 8051 was a very simple machine, with a limited instruction set. The DS87C550 provides an extension of the original 8051, while maintaining compatibility with the original 8051 (i.e. the DS87C550 executes 8051 programs with the same effect as the 8051). The extension concerns the data pointer register of the original 8051. The original 8051 had a single data pointer register DPTR. The DPTR register is used in MOVE instructions to move data between register and memory locations. The DPTR contains an address that the processor uses to address memory [is] used in the MOVE instructions. Data from a succession of addresses can be moved to register and processed by executing successive MOVE instructions, each followed by incrementation of the address in the DPTR register."

The paragraph beginning on page 1, lines 18-22 has been amended as follows:

"The 8051 had a DPTR increment instruction INC for incrementing the DPTR. But the 8051 did not have the [no] possibility to decrement the DPTR. The DS87C550 improves this. The DS87C550 introduces an instruction-settable control bit which controls whether the processor responds to the 8051 DPTR increment instruction by incrementing the DPTR or by decrementing the DPTR."

The paragraph beginning on page 1, line 23 to page 2, line 2 has been amended as follows:

"The original 8051 only had a single DPTR register. If the original 8051 had to transfer data from a first series of memory locations to a second series of memory locations with MOVE instructions, the address in the DPTR register had to be replaced alternately with an address for addressing the first series and an address for addressing the second series. This caused considerable instruction overhead. The Dallas [DS86C550] DS87C550 reduces this overhead. Two registers are provided instead of the single DPTR, one register for addressing memory in moves to memory and one for move from memory. In a toggle mode, the [DS86C550] DS87C550 uses alternately one register and the other, e.g. in MOVE or INC instructions."

The paragraph beginning on page 4, lines 18-24 has been amended as follows:

"The fourth instruction causes the processing device to move a value of 2 into the selector register. This value causes the processing device to receive the second address when a value is loaded subsequently into the data pointer register DPTR. The [third] fifth instruction commands the move of an address value A1 to the data pointer register DPTR. Because the selector register has been set to 2, the processing device will use this address value [A2] A1 as the second address. Subsequently, the processing device will use alternately the first and the second address (updated if necessary) when memory access instructions refers to the DPTR."

The paragraph beginning on page 5, lines 11-17 has been amended as follows:

"In operation the execution unit 10 executes a sequence of instructions. Each time that such an instruction refers to a data pointer register for specifying a memory address for memory access, the execution unit supplies an address enable signal on the address enable output to the address selector circuit. The register selector register 128 controls which one of the registers 120, 122 receives this address enable signal. This control is effect via the AND gates 124, 126. The enabled register 120, 122 will supply its content as an address to the address output of the processing device."

The paragraph beginning on page 7, lines 1-11 has been amended as follows:

"Of course, implementation of the invention is not limited to the embodiment shown in figure 1. For example, instead of connecting both registers to the address output and enabling different ones of these registers 120, 122, one may [use] place these registers in a circular shift register arrangement. In this shift register arrangement the content of the first register 120 is loaded into the second register 122, and the old content of the second register 120 is loaded into the first register 120 each time after the execution unit 10 supplies an address enable signal. Thus, only the first register 120 needs to be connected to the address output and the content of the first register is always output in case of an address enable signal. Updates are also applied only to the content of the first register 120, the type of update preferably being dependent on content of the control register for the particular address that is in the first register 120."

The paragraph beginning on page 12, lines 1-12 has been amended as follows:

"A data processing device has load and store instructions which address memory with the content of a data pointer register. In a normal mode, the same data pointer register is used for all load and store instructions. In this mode the processor is compatible with a older processor design. In a special mode, at least two different registers are used alternately to address memory when memory access instructions are executed. A control register controls whether or not the different registers are updated as part of the memory access instructions. Preferably, the control register provides for more than one different kind of update of the different registers, such as post addressing increment, post addressing decrement etc.

[Fig. 1]"

IN THE CLAIMS

Claims 1-5, 8 and 9 have been amended as follows:

1. (Amended) A data processing device, comprising

[-] a register circuit for storing at least two addresses in parallel;

[-] an address selector including a register selector register and a logic circuit collectively arranged to cycle through a set of states in which respective ones of the at least two addresses become a currently selected address [respectively];

[-] an instruction execution unit having an instruction set that contains a memory access instruction, execution of the memory access instruction causing the instruction execution unit to issue memory access signals with an access address determined from the currently selected address, execution of the memory access instruction further causing the address selector to cycle to a next one of the states[,]; and

[-] a control register in communication with said register selector register and said logic circuit, said control register [that is] being instruction-settable to respective control states that control whether or not the processing device updates the at least two addresses [will be updated] as a side-effect of executing the memory access instruction.

2. (Amended) [A] The data processing device as claimed in claim 1, wherein each control state specifies respective update actions for all of the at least two addresses.

3. (Amended) [A] The data processing device as claimed in claim 1, wherein the control states [comprise states] specify a choice from at least no-update, update by incrementing with a predetermined value and update by decrementing with the predetermined value [respectively].

4. (Amended) [A] The data processing device as claimed in claim 1, wherein the execution of said memory access instruction further causes the instruction execution unit to perform, upon the currently selected address, the update action that is specified by the control state of the control register for that one of the at least two addresses that is the currently selected address.

5. (Amended) [A] The data processing device as claimed in claim 1, wherein the instruction set [comprising] includes a load from memory instruction and a store to memory instruction[, both] for causing the instruction execution unit to respond [as claimed for] to the execution of said memory access instruction

8. (Amended) [A] The data processing device as claimed in claim 1, wherein the address selector [cycling] cycles back and forth between states that select a first and second one of the at least two addresses respectively.

9. (Amended) [A] The data processing device as claimed in claim 1, wherein the register circuit [storing] stores at least three addresses, and the address selector [cycling] cycles through a series of at least three states that select different ones of the at least two addresses.